Overview:

The automatic gain control (AGC) section adds gain to maintain a fairly constant output signal level. This reduces the amount of signal level variation at the output of the part and, therefore, reduces the number of bits that must be carried in any post processing. In the ISL5416, the AGC follows the channel filtering. This means that all of the gains through the NCO, mixer, and FIR filter sections are fixed gains and do not induce AM distortion before the large interfering signals can be filtered out. If large interfering signals are not filtered prior to the AGC, the gain adjustments by the AGC can AM modulate the large signals and cause AM sidebands to fall inside the frequency band of interest.

A block diagram of the AGC is provided in figure 2. The main components are a forward gain stage and a loop filter. The AGC in the ISL5416 is an AGC loop where the level at the output of the AGC is measured and used to adjust the gain through the AGC. The forward path adds gain to the FIR2 filter outputs before sending the data to the back end filters and output section. The loop filter measures the level at the output of the forward path and adjusts the forward path gain to maintain the programmed output. The ISL5416 AGC also includes a programmable delay and a set of timers is provided for tuning the AGC response and for aligning the gain adjustments to system timing.

The forward path gain is divided between a barrel shifter and a multiplier. An 18-bit gain word controls both blocks. The most significant 4 bits control the barrel shifter, which adds gain in 6 dB steps over a 0 to 90 dB range. The other 14 bits are appended to a fixed 0x01b and control a 16-bit multiplier gain. The multiplier gain can range from 1.0 to almost 2.0 and provides fine gain steps between the coarse steps of the barrel shifter. Figures 1A and 1B show the overall gain response in dB versus the 18-bit control word value. Overflow detection and limiting is provided in the I and Q forward paths to saturate the output if the gain causes it to exceed full scale.
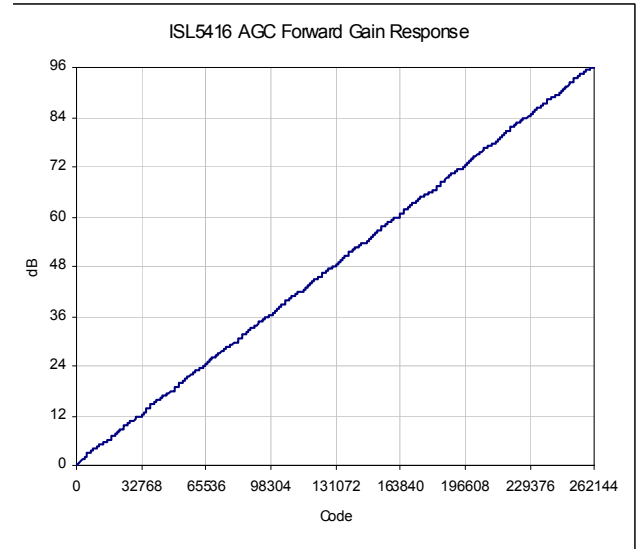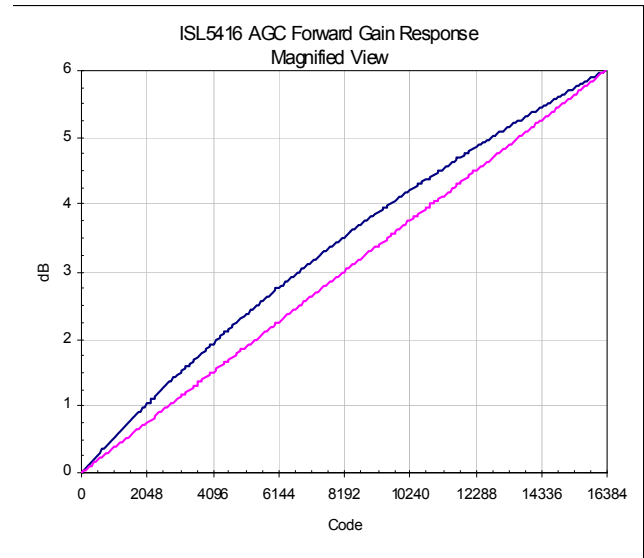

FIGURE 1A. AGC FORWARD GAIN

FIGURE 1B. MAGNIFIED VIEW

FIGURE 2. AGC BLOCK DIAGRAM

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The loop filter includes an error detector, error scaling, integrator (accumulator), gain range limits, and processor control and monitoring circuitry. The error detector first converts the I/Q samples at the forward path output to a magnitude samples. The magnitude is then subtracted from a user programmable set point value to compute the error signal. The error is scaled and integrated. The error scaling, or loop gain, is programmable and sets the loop response. The integrator (accumulator) low pass filters the error. The output of the integrator is the control word for the forward path gain. If the forward path output is larger than the set point, the error is negative, and the gain is reduced; if the forward path output is smaller than the set point, the error is positive, and the gain is increased. There are programmable gain range limits on the integrator (accumulator) to restrict the AGC to a range smaller than 96 dB range provided. Note that the AGC can only add gain to the signal.

The magnitude computation uses a multi-cycle implementation of the CORDIC algorithm, computing one cycle (rotation) per clock. The accuracy of the magnitude computation depends on the number of cycles. There is a gain in the computation due to the rotation vectors. The user must account for this gain when computing the set point and the loop gain. Table 1 gives the magnitude accuracy and gain versus the number of compute cycles.

TABLE 1. MAGNITUDE ACCURACY, GAIN VS. CLOCK CYCLES

COMPUTE CYCLES	ERROR (±)	GAIN (dB)
2	0.48	1.581
4	0.03	1.642
8	0.00013	1.647

There are two settling modes provided for the loop. The mean settling mode, described above, makes adjustments to the gain based on the size of the magnitude error and the error scaling value or loop gain. Since the adjustment is proportional to the error, as the error decreases, the size of the adjustment decreases. This causes the loop gain to asymptotically approach the final gain value. Since the adjustments go to very small values, the AM distortion after settling is minimized. The other settling mode is the median mode. In this mode, the sign of the magnitude error is used to determine whether a fixed value, scaled by the loop gain, is added or subtracted from the accumulator. In this mode, the loop settles to where half of the error samples are positive and half are negative. This mode can settle faster because the adjustment value is constant. However, after settling, the loop still makes the same size adjustments and may have excessive AM distortion.

In both settling modes, the error signal is scaled by the loop gain value. There are separate loop gain values for positive and negative errors. This feature can be used to make the loop respond differently to arriving and departing signals. For example, the loop can be programmed to quickly reduce the gain when large signals appear (attack) but to slowly increase the gain when a signal goes away (decay) in anticipation of a new transmission. Asymmetric gain adjustment can also be used to compensate for the asymmetric error range when the set point is at a value other than half scale.

The user can load two sets of loop parameters (attack and decay loop gains and settling mode) at once. Selection between the two sets of parameters can be under manual (uP) control or can be under the control of the timers mentioned above to automatically align the parameter selection to system timing. Among the possible uses for parameter switching are such things as fast loop/slow loop, adapt/track, adapt/hold, and median settling/mean tracking.

The forward gain can be loaded and read by the uP. The gain value is loaded into the accumulator by first writing the gain value to a holding register and then transferring the gain to the accumulator. The transfer can be done either by a write to an indirect address location or, if enabled, by a SyncIx signal. If the value that is loaded is outside the gain limits, the accumulator will be set to the limit and begin its adjustments from there. If both limits are the same, the AGC will hold that value. If the load value is within the limits and the loop gain is zero, the loop will hold the load value. To read the gain, the uP first writes to an indirect address to sample the gain synchronous to the clock and stabilize it for reading. It is then read via the sequenced read mode at direct addresses 4-7.

The gain can be routed to the output section for real time monitoring. The user has the choice of the real time gain value or the gain sampled by the indirect uP write (dhd-check). The AGC gain is aligned with the data sample if the back end is bypassed. The AGC gain is not interpolated or resampled to match the I/Q delays when the backend section is used.

Modes and Loop Response

There are three main AGC loop update modes and two variations. The three modes are continuous, timed, and sampled and have to do with the way the loop gains are selected and the forward gain is updated. For the continuous and timed modes the user can divide the forward path into delayed and non-delayed paths with the non-delayed path routed to the loop filter and the delayed path to the output. The forward gain is applied to the samples as they exit the delay. This allows the gain for an output sample to be based on the samples both before and after it. Note that for the sampled mode, the split path is always present. The AGC

can also be bypassed entirely. The minimum number of clocks between samples into the AGC is mode dependent and is given in table 2.

TABLE 2. REQUIRED INPUT SAMPLE SPACING VS. MODE

MODE	MINIMUM INPUT SPACING (CLOCKS)
BYPASS	1
CONTINOUS	2
CONTINOUS W/ DELAY	4
TIMED	2
TIMED WITH DELAY	4
SAMPLED	4

FIGURE 3. CONTINOUS MODE

CONTINOUS MODE:

In the continuous mode, the loop is updated on a sample by sample basis. The loop gain and settling mode selection is controlled directly by the uP. Block diagrams for the loop architecture for the continuous mode with and without the programmable delay are shown in figures 3 and 4. Figures 6A through 6E show the loop response to a 6 dB change in a CW input. For this example, there is minimal filtering of the CW signal in the modulator and CIC, halfband, and RRC filtering in the ISL5416. The input sample rate to the ISL5416 is 61.44 MSPS and the output sample rate is 7.68 MSPS. Figure 5 shows the test configuration. All four channels of the ISL5416 are used. Channel 3 has a fixed gain and channels 2, 1, and 0 have loop gains of ~0.25, ~0.5, and ~1.0 dB/sample for an error value of one-half of full scale. The AGC set point is -12 dBFS. Mean settling mode is selected. Figure 6A shows the I outputs of channels 3 and 1, figures 6B and 6D show the magnitude (computed in post processing) for all four channels, and figures 6C and 6E show the AGC gain for all four channels.
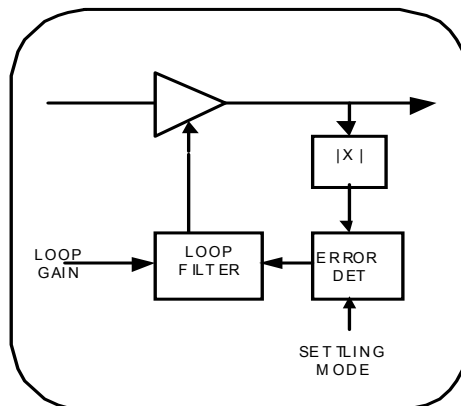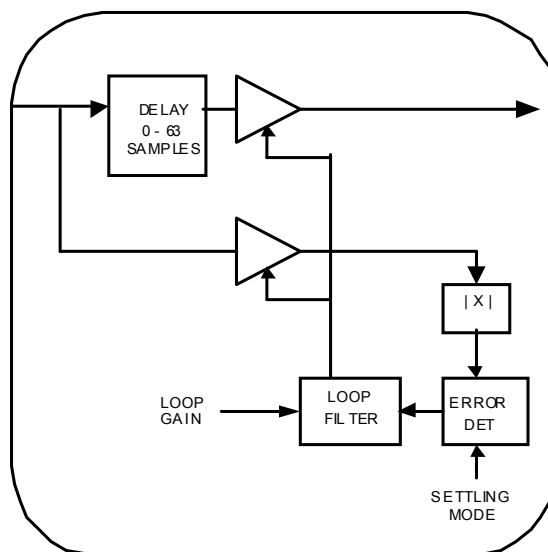
FIGURE 4. CONTINOUS MODE WITH DELAY
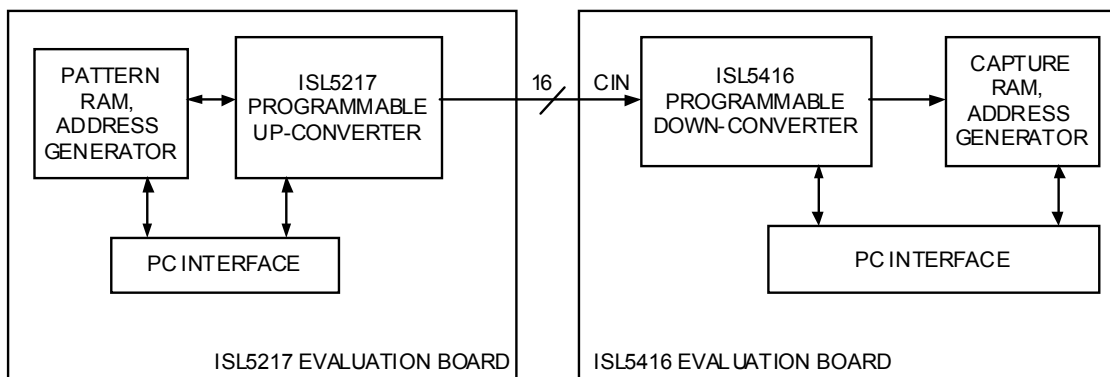
FIGURE 5. TEST CONFIGURATION
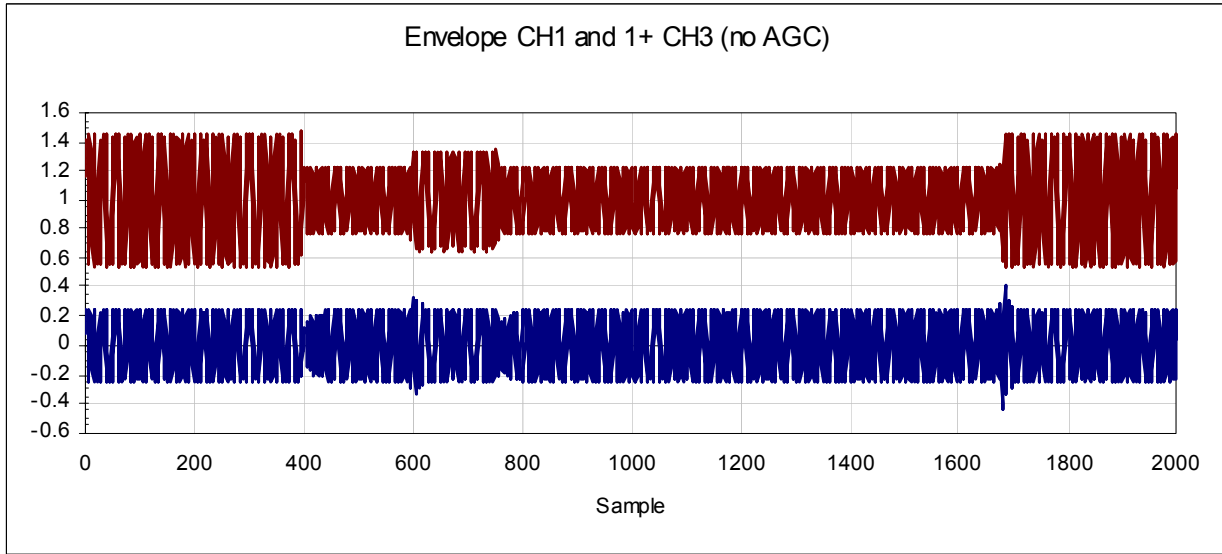
FIGURE 6A. I OUTPUT WITH AND WITHOUT AGC
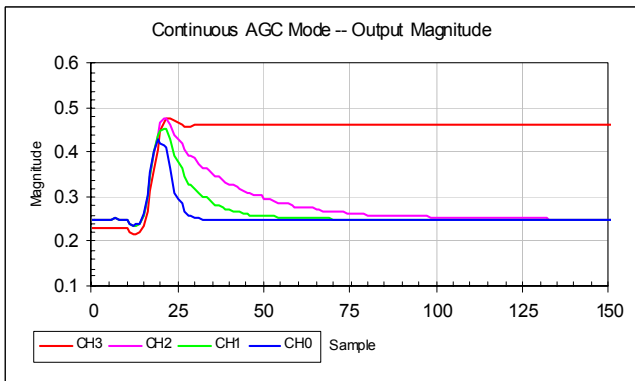
FIGURE 6B. INCREASING INPUT POWER
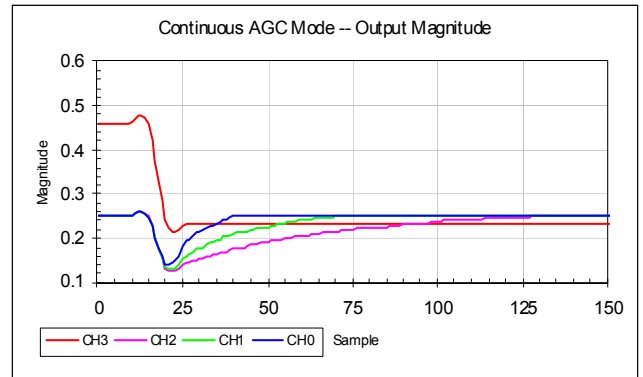
FIGURE 6D. DECREASING INPUT POWER
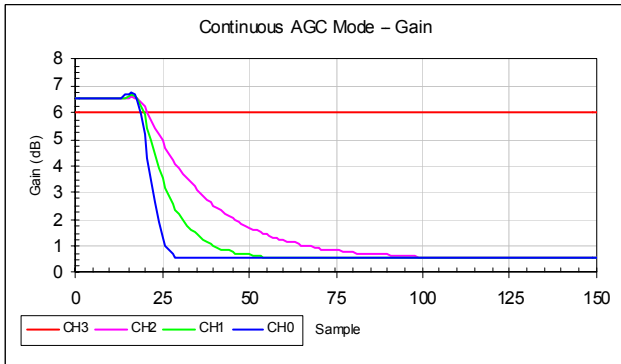
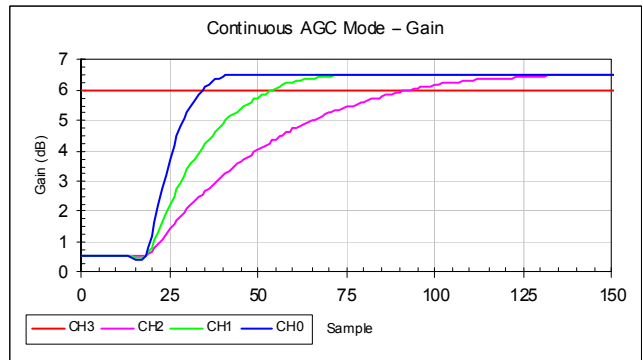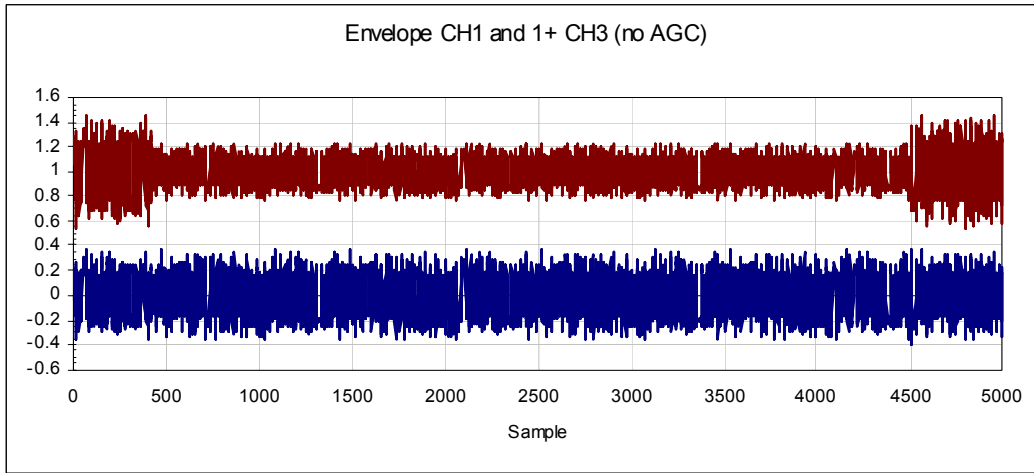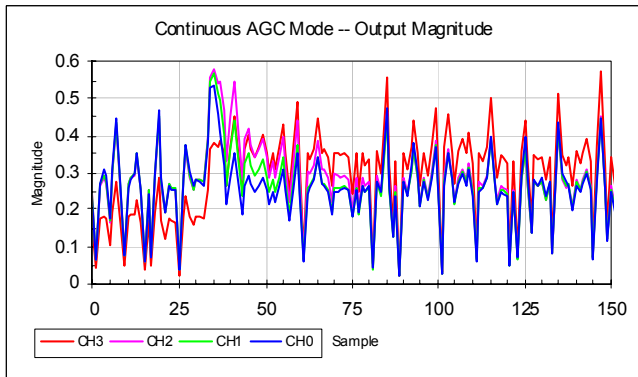
FIGURE 6C. INCREASING INPUT POWER

FIGURE 6E. DECREASING INPUT POWER

CONTINOUS MODE - FILTERED QPSK DATA:

These plots show RRC filtered transmit data with CIC, HBF, and RRC filtering in the receiver. The data is a 511 bit sequence on I and Q with a 6 dB change after 2044

symbols. The symbol rate is 3.84 MSym/sec and the output is at 2x the symbol rate. The loop gains are the same as for the CW continuous case.

FIGURE 7A. I OUTPUT WITH AND WITHOUT AGC

FIGURE 7B. INCREASING INPUT POWER
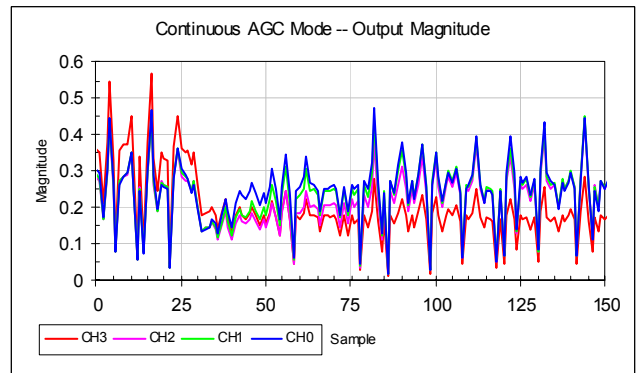
FIGURE 7D. DECREASING INPUT POWER
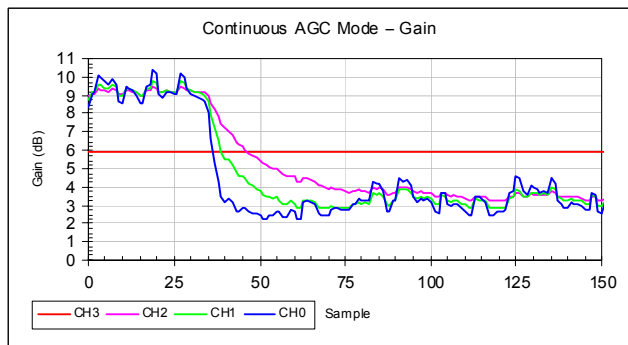
FIGURE 7C. INCREASING INPUT POWER
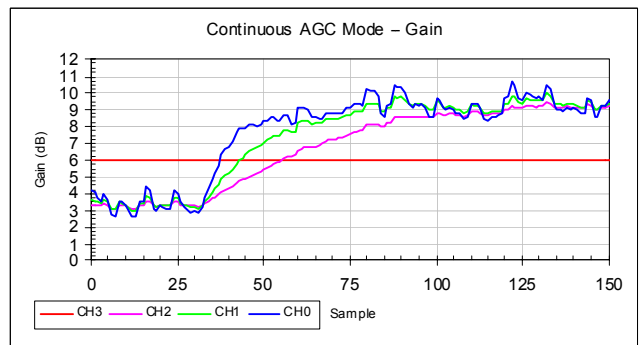
FIGURE 7E. DECREASING INPUT POWER

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As expected, the higher loop gains settle faster but the lower loop gain case has a more stable gain.
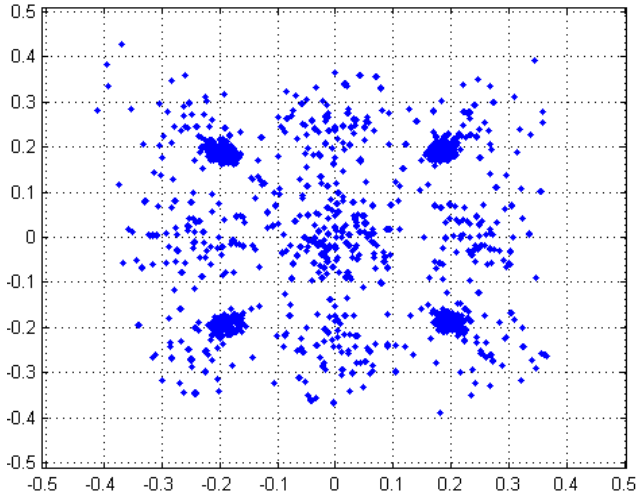
FIGURE 7F. I/Q DISPLAY WITH AGC (8192 SAMPLES AT 2 SAMPLES PER SYMBOL)
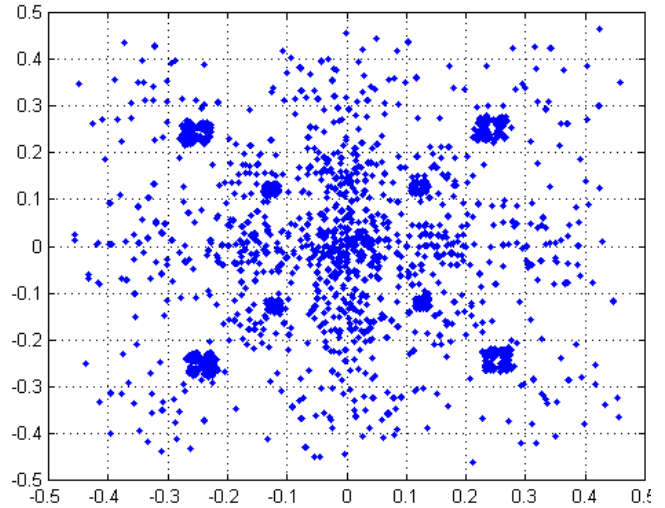
FIGURE 7G. I/Q DISPLAY WITHOUT AGC (8192 SAMPLES AT 2 SAMPLES PER SYMBOL)

CONTINOUS MODE WITH DELAY:

These examples have the same loop gains as the continuous mode example. The programmed delays are 20, 10, and 5 samples for channels 2, 1, and 0, respectively.
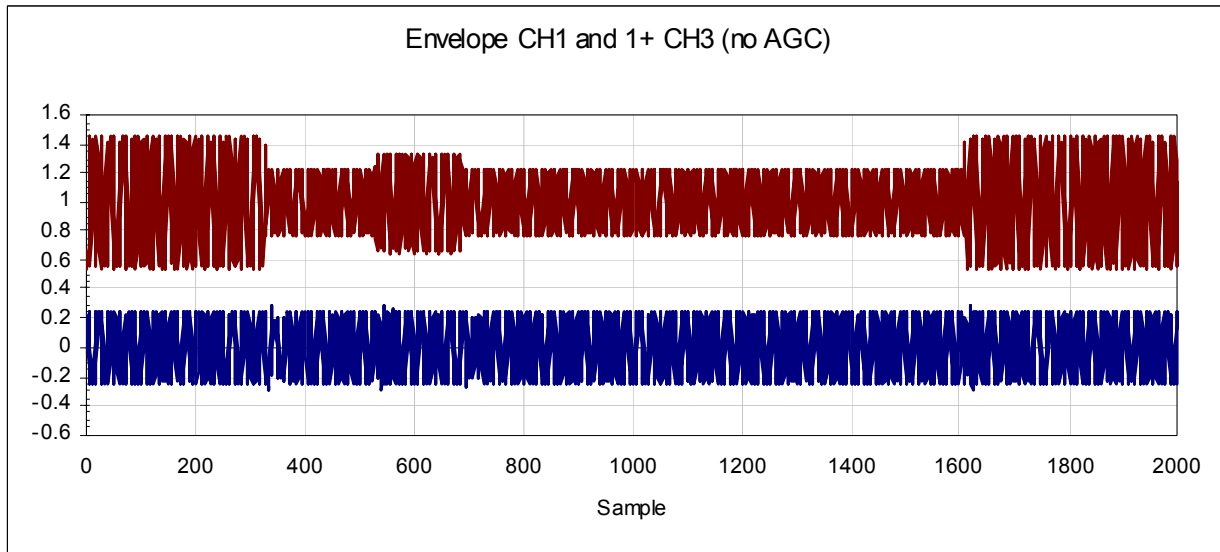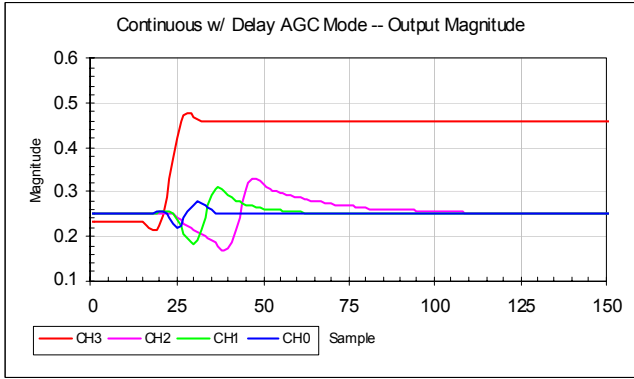

FIGURE 8A. I OUTPUT WITH AND WITHOUT AGC

Continuous w/ Delay AGC Mode -- Output Magnitude

FIGURE 8B. INCREASING INPUT POWER

Continuous w/ Delay AGC Mode -- Gain

FIGURE 8C. INCREASING INPUT POWER

Continuous w/ Delay AGC Mode -- Output Magnitude

FIGURE 8D. DECREASING INPUT POWER

Continuous w/ Delay AGC Mode -- Gain

FIGURE 8E. DECREASING INPUT POWER

The size of the AGC loop transient due to a change in gain at the input depends on both the loop gain and the settling mode. Setting the loop gain is a trade off between setting time and stability of the gain with transients due to noise and/or data. Adding delay can minimize the peak excursions at the output. The delay causes the AGC to start to settle to the new gain before the power changes exits the delay, a response similar to a feed-forward AGC architecture. The added delay causes the gain transient to be divided into a positive and a negative transient, each with about half the peak-to-peak transient. While the peak-to-peak amplitude of the transient is about the same as without the delay, the amount of time the output of the AGC is in saturation or falls below the output LSB is reduced. The amount of delay that is needed depends on the loop gain and the peak gain change expected.
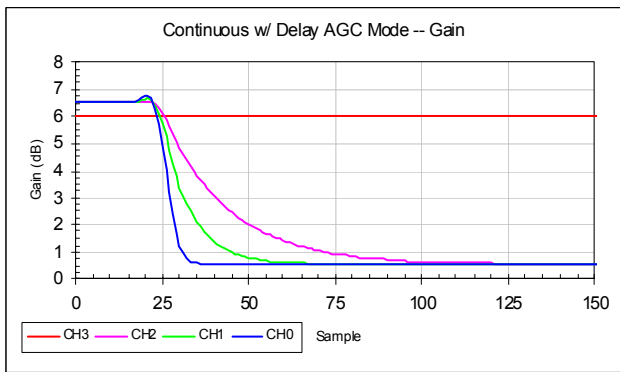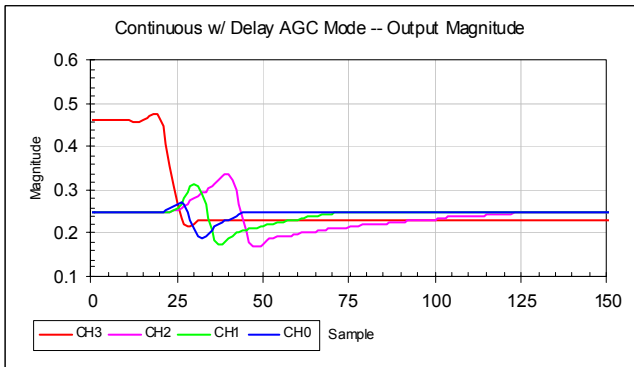
TIMED MODE:

The timed mode uses a set of counters to change the loop gain and/or settling mode of the loop at periodic intervals. This mode is intended for TDMA applications where there are defined time slots and the gain may vary greatly from one time slot to the next. While the control microprocessor could control the gain and mode selection, counter control can eliminate processor timing constraints and reduce processor loading. The counters select one of two sets of loop gains and/or settling modes. Typically the timing would be programmed to select a high loop gain for the guard time and beginning of a new time slot to rapidly settle to right gain for the new user. After allowing sufficient time for settling, a lower (or zero) loop gain would be selected for the main part of the slot.

A block diagram of the three counters is provided in figure 9. All are updated at the clock rate. The slot counter is programmed to count out the time slot period, reload, and start the delay counter. The Synclx signal can start or reload the slot counter to align it to system timing. The delay counter starts when the slot counter loads/reloads. It is used to compensate for delay through the filters preceding the

AGC or other system delays. The third counter is the interval counter and selects the loop parameters. The interval counter loads when the delay counter finishes its count. When the interval counter finishes its count, it disables itself and waits for the next start signal from the delay counter. Loop gain and settling mode 1 are used in the loop filter while the interval counter is active and loop gain and settling mode 2 are used when the interval counter is disabled.

All of the counters are 16 bits which allowing a time slot length, delay, and interval up to 819 usec with an 80 MHz clock. The interval count must be less than the slot length, but since the delay can be up to a time slot, the interval can extend past the end of the slot counter period. The timing is illustrated in figure 10 below.
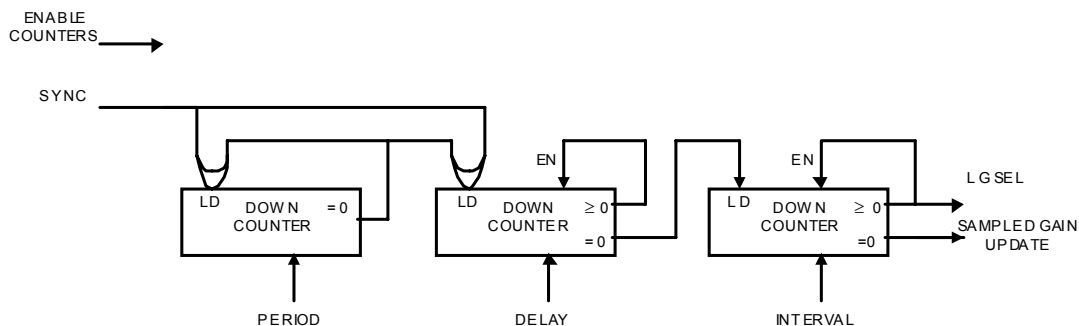
FIGURE 9. AGC COUNTERS
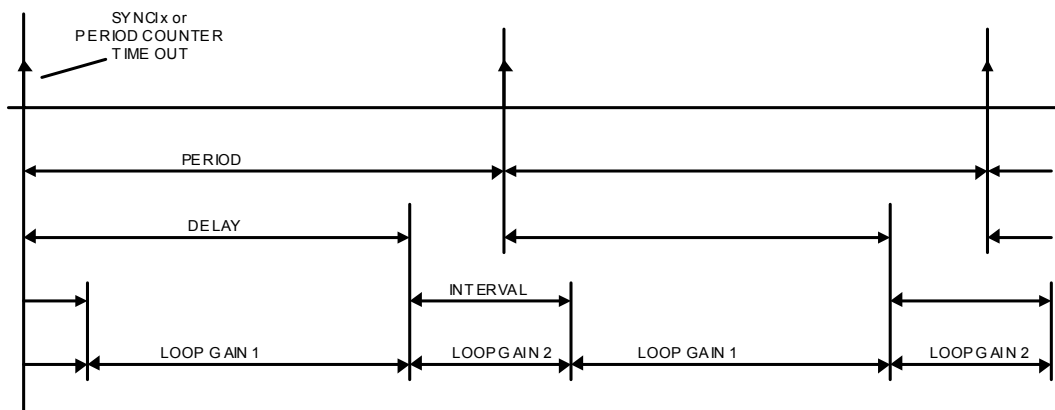
FIGURE 10. TIMED AGC MODE

The AGC is allowed to adjust at the slot boundaries. The signal amplitude changes 6 dB at the slot boundaries and by approximately 3 dB within the time slot.
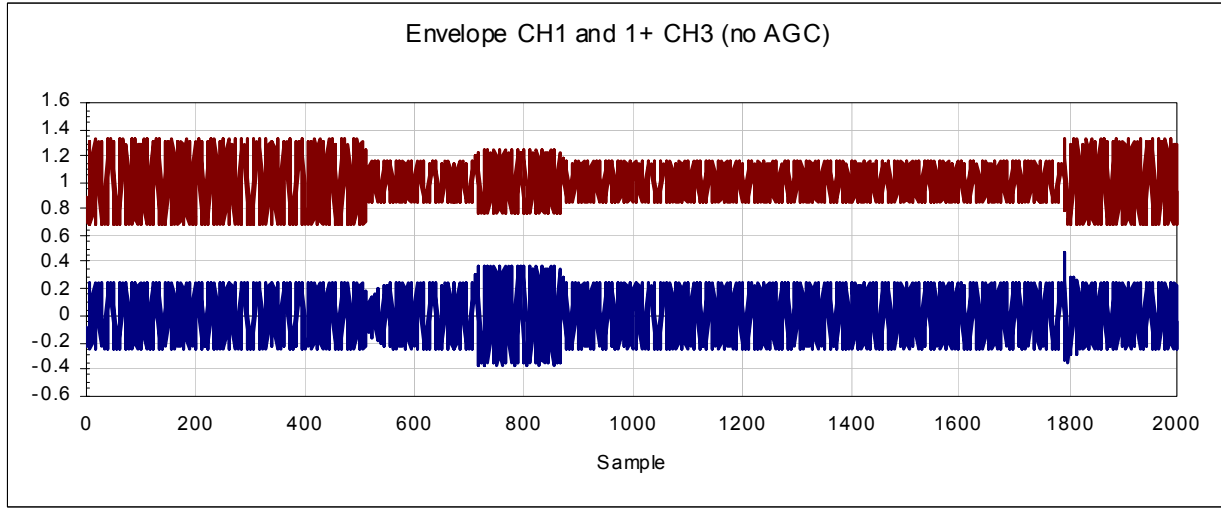
FIGURE 11A. I OUTPUT WITH AND WITHOUT AGC
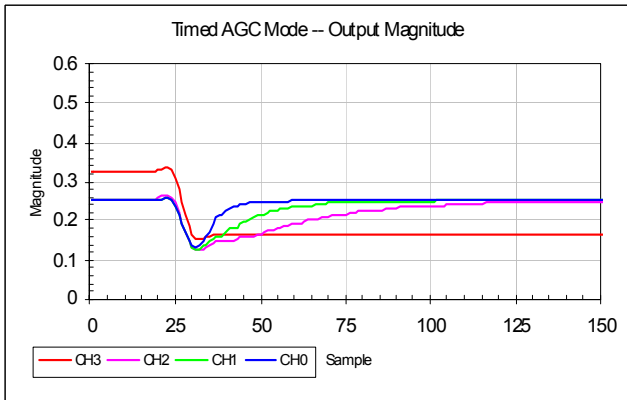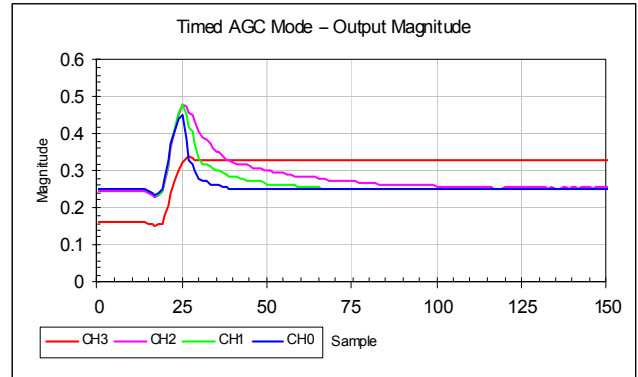

FIGURE 11B. INCREASING INPUT POWER

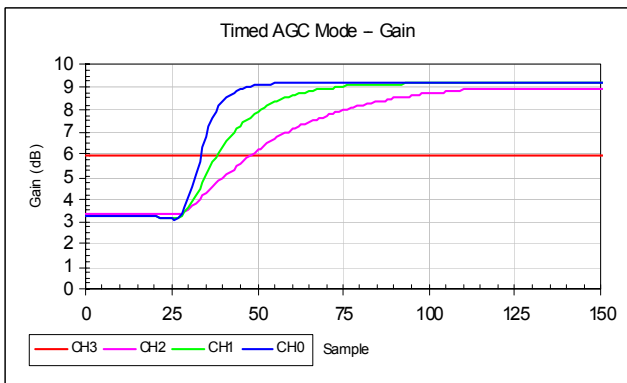**FIGURE 11D. DECREASING INPUT POWER**
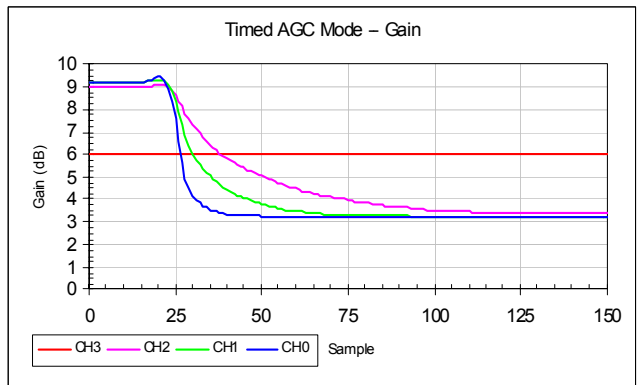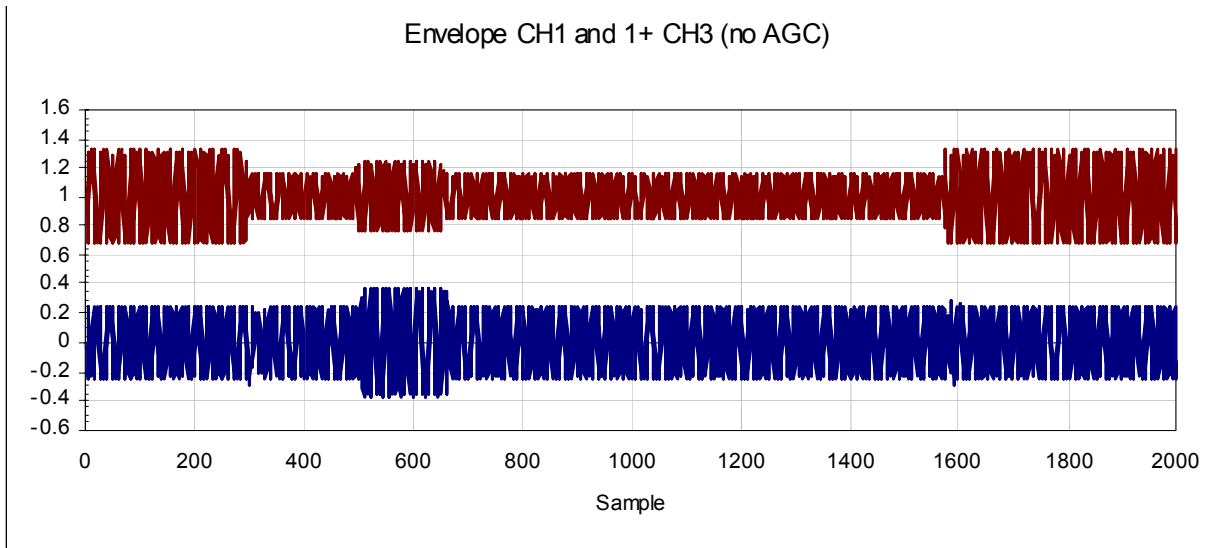

FIGURE 11C. INCREASING INPUT POWER

FIGURE 11E. DECREASING INPUT POWER

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TIMED MODE WITH DELAY:

The programmable delay can be used to bias the timing so that the guard time is largely ignored and the high gain interval enabled at with the first samples of the new slot. If the delay is set equal to the guard time, the high gain will be enabled when the first samples of a new slot enter the delay

line and last samples of pervious slot exit the delay. The loop adapts to the new signal level while the first samples of the new slot are in the delay line and settles to within a smaller uncertainty by the time the samples exit the delay.
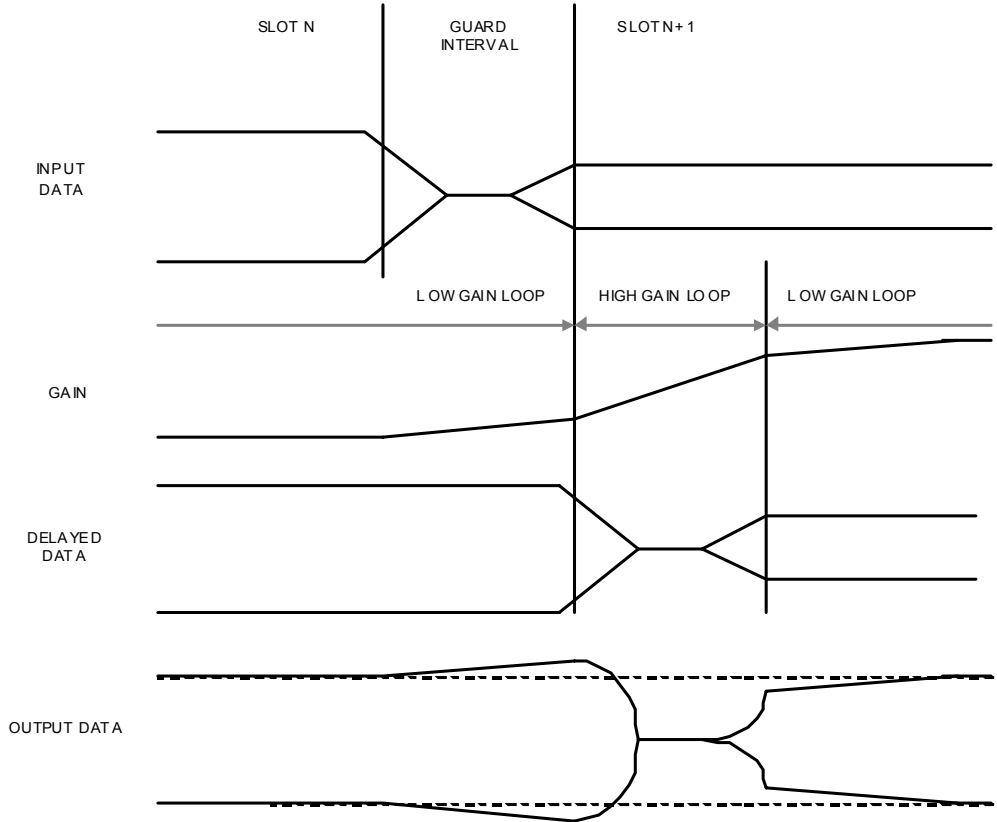
**FIGURE 12. THE EFFECTS OF DELAY ON A TIMED AGC
LOOP IN A TDMA SYSTEMS**

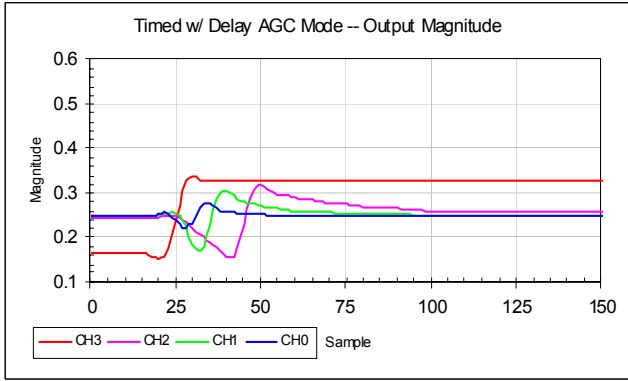

FIGURE 13A. I OUTPUT WITH AND WITHOUT AGC

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FIGURE 13B. INCREASING INPUT POWER
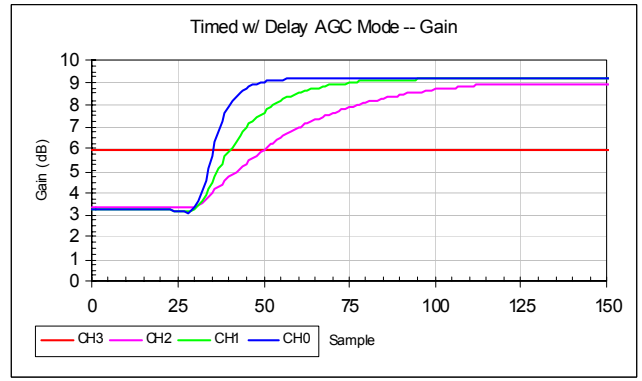

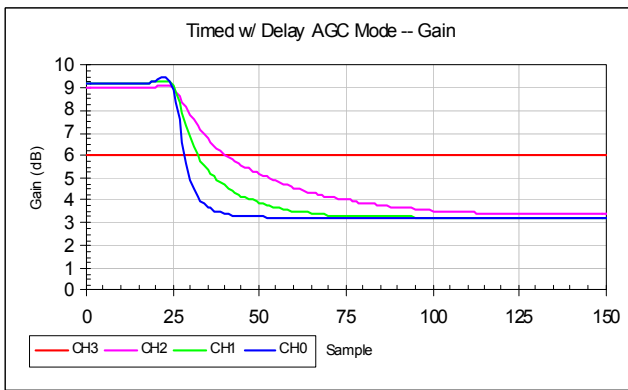**FIGURE 13C. INCREASING INPUT POWER**

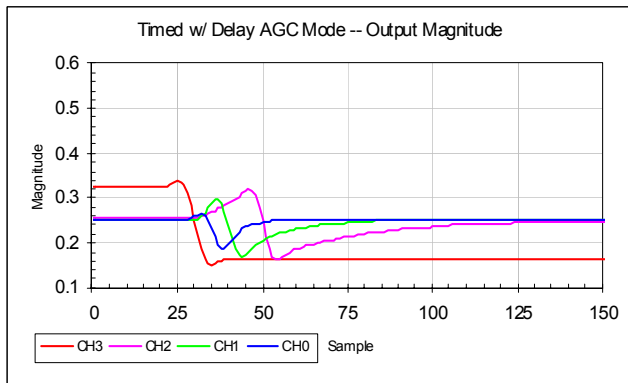**FIGURE 13E. DECREASING INPUT POWER**

FIGURE 13G. DECREASING INPUT POWER

Reading the AGC gain

There are several ways to obtain the AGC gain value. One is a uP sampled mode where the uP writes to IWA 0x*010h to sample the gain and stabilize it for reading and then reads the data via the sequenced read port at direct addresses 4-7. The AGC gain is also available "real time" through the parallel outputs, serial outputs, and the sequenced read port. This "real time" output can either be the gain word updated at every sample through the AGC or the gain word can be sampled and held by the AGC counters. The sampled-and-held version is output with each new I/Q output sample, but its value only changes when updated by the counters. A block diagram of the AGC is included below (Figure 14).
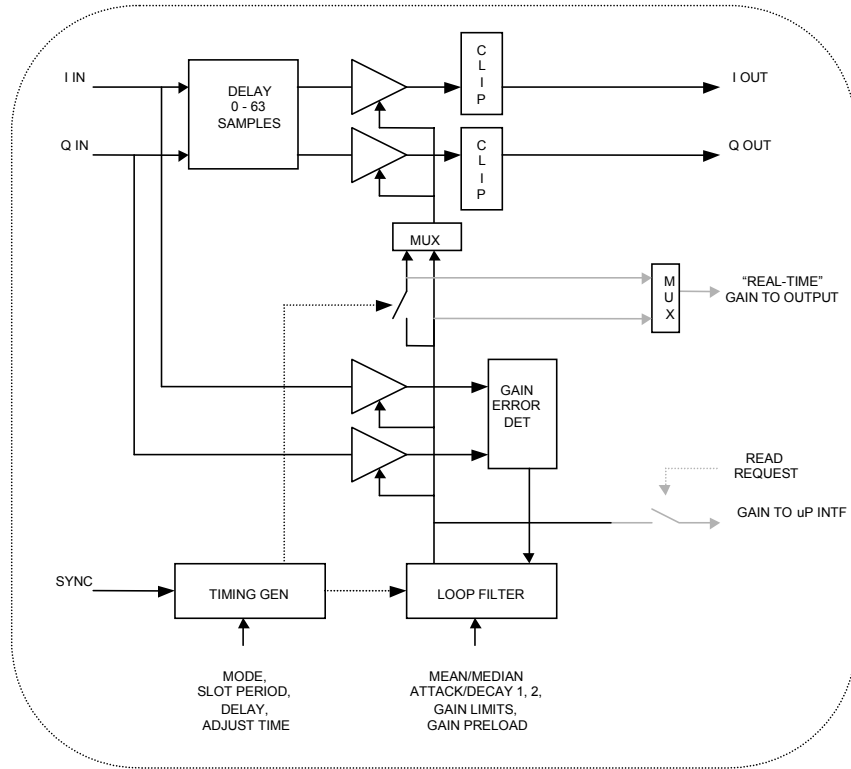
FIGURE 14. CONCEPTUAL AGC BLOCK DIAGRAM

Notes:

The "real-time" gain is provided to the parallel output, serial output, and sequenced read uP outputs. The sampled or requested read gain is only available at the sequenced read on the uP interface.

Note that the "real-time" gain can be either the gain from the loop filter or the sampled gain from the loop filter. Though the sampled gain was intended for the sampled AGC mode, it will update in the timed mode when the duration counter reaches zero. This update can be aligned to the time slots, allowing the AGC gain to be sampled and held at the same time each slot whether or not the sampled AGC mode is used.

GAIN OUTPUT FORMAT:

The gain output is a floating point value with a 4-bit exponent and a 12-bit mantissa. A leading 0x01b is suppressed for the mantissa.

The bits are:

$G = E\ E\ E\ E\ M\ M\ M\ M\ M\ M\ M\ M\ M\ M\ M\ M$

The bits are converted to linear gain by the equations:

$LINGAIN = (1.0 + M/2^{12}) * 2^{E}$.

The bits be converted to log gain by:

$LOGGAIN = 6.02 * G/2^{12}$.

This is not exactly linear in dB (see the AGC operation description) and has a positive bias with a peak error of +0.5 dB. The bias can be removed by subtracting 0.25. To convert this from gain to RSSI, the G value can be inverted (ones complement should be sufficient) and an offset added.

The LOGGAIN error can be reduced to <0.1 dB by using the equation:

$LOGGAIN = 6.02 * E + [-8 * (M/2^{13})^{2} + 24 * (M/2^{13}) - 10]$.